# Session 18 Overview

# Clock and Data Recovery

**Chair: Roger Minear,** Wyomissing, PA

**Associate Chair: Bob Payne,** Texas Instruments, Dallas, TX

Applications for multi-Gb/s serial-link technology are expanding beyond optical and backplane communications to memory and chip-to-chip interconnect. As a result, clock- and data-recovery (CDR) circuits are needed that combine high-speed performance with low cost, low power, and smaller area. In addition, applications in passive optical networking (PON) and low-latency memory interfaces require that CDR lock-time improves beyond what is possible using widespread dual-loop CDR architectures.

The 8 papers in this session represent a cross-section of recent advances in CDR techniques, ranging from compact 25Gb/s receivers for high-density interconnects to low-power delay-locked loops (DLLs) for 300MHz DDR timing generation. Applications involving high-speed serial memory interfaces are also included.

In Paper 18.1, a compact 25Gb/s phase interpolator-based CDR in 90nm CMOS occupying only 0.09mm$^2$ is described. The low power (< 4mW/Gb/s), high speed, and compact area lead towards higher levels of integration and higher-density interconnections.

Optical networking applications place strict demands on jitter tolerance and recovered-clock quality. In Paper 18.2, the application of a mixed-signal filter to a CDR is covered. It can be used across a wide range of SONET data rates (OC-3 to OC-48).

As memory bandwidths increase and server applications demand larger capacities, CDR circuits become necessary in memory interfaces. Two papers in this session address techniques to enhance memory system performance. A DLL used for phase alignment and duty-cycle correction for DDR interfaces is described in Paper 18.3. An advanced memory buffer (AMB) with a fast-locking CDR for next-generation fully buffered DIMM standards is presented in Paper 18.6.

The authors of Paper 18.4 explore different methods of phase estimation that are enabled by changes to the phase-control logic of a dual-loop CDR. Three such designs are described which offer improvements in lock time, frequency tracking, and jitter tolerance.

In Paper 18.5, a hybrid of a traditional phase-tracking CDR combined with blind-oversampling is shown to improve low-frequency jitter tolerance by 32x over phase-tracking alone.

In Paper 18.7, a 0.13µm CMOS 10Gb/s receiver that uses a 2.5GHz clock and a quarter-rate linear phase detector to meet OC-192 jitter-tolerance requirements, is detailed.

The 20Gb/s transceiver in Paper 18.8 showcases a quarter-rate bang-bang phase detector that uses a phase summer to replace a digital early-late vote counter.

 

**18.1 A 25Gb/s CDR in 80nm CMOS for High-Density Interconnects** **1:30 PM**

*C. Kromer,* ETH Zürich, Zürich, Switzerland

A CDR for source-synchronous high-density link applications receives 25Gb/s at a BER of $<10^{-12}$. The CDR is a first-order bang-bang topology employing a phase interpolator, linear half-rate phase detector, an analog filter followed by a limiter and a digital loop filter. The core CDR circuit occupies $0.09mm^2$ and consumes 98mW from a 1.1V supply.

**18.2 A 2.5Gb/s Multi-rate 0.25µm CMOS CDR Utilizing a Hybrid Analog/Digital Loop Filter** **2:00 PM**

*M. Perrott,* MIT, Cambridge, MA

A CDR comprises a Hogge detector and a $1^{st}$-order $\Delta\Sigma$ ADC, and uses a hybrid analog/digital loop filter to enhance integration and allow bandwidth tuning over a wide range of data rates from 155Mb/s to 2.7Gb/s. The CDR exceeds SONET performance at relevant data rates and generates $1.2ps_{rms}$ jitter at 2.5Gb/s.

**18.3 A 0.03mm² 9mW Wide-Range Duty-Cycle-Correcting False-Lock-Free DLL with Fully Balanced Charge-Pump for DDR Interface** **2:30 PM**

*Y. Tokunaga,* Matsushita, Moriguchi, Japan

A duty-cycle-correcting false-lock-free DLL for DDR interface is proposed. A fully balanced charge-pump equalizes the charge and discharge pulses of the phase detector to reduce update noise. The DLL achieved 49% to 51% duty-cycle output from a 30% to 70% duty-cycle input clock operating from 20 to 300MHz, consumes 9mW from a 2 to 4V supply, and occupies $0.03mm^2$ in a 0.30µm CMOS process.

**18.4 Improving CDR Performance via Estimation** **3:15 PM**

*H. Lee,* Stanford University, Stanford, CA

A dual-loop CDR can be viewed as a simple phase-estimator. Different estimators can be built by changing the phase DAC control logic. Three different 0.13µm estimators for a 3Gb/s serial link are presented. These estimators address dual-loop CDR limitations including lock time, frequency range, and jitter tolerance in non-mesochronous systems.

**18.5 A 3.2Gb/s Semi-Blind-Oversampling CDR** **3:45 PM**

*M. van Ierssel,* University of Toronto, Toronto, Canada

A hybrid CDR increases jitter tolerance of a phase-tracking CDR by a factor of 32 at low frequencies, while maintaining the high-frequency jitter tolerance of a 5× blind-oversampling CDR. Measurements on a 0.11µm CMOS test chip at 2.4Gb/s confirm a $200UI_{pp}$ jitter tolerance at 200kHz. At 2.4Gb/s, the chip consumes 180mW from a 1.2V supply.

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**18.6 Data Recovery and Retiming for the Fully Buffered DIMM 4.8Gb/s Serial Links** **4:15 PM**

*H. Partovi,* Infineon, San Jose, CA

Data recovery and retiming of 4.8Gb/s fully buffered DIMM serial links are described. A 2.4GHz retiming FIFO with an integrated insertion MUX is used to minimize the thru-latency. Fabricated in a 0.13µm 1.5V CMOS technology, the chip occupies $9.2\times4.5mm^2$. Using wide-band CML techniques, the input sensitivity with a minimum eye-opening of 0.35UI, is better than $50mV_{p-p}$ at a BER of $10^{-12}$.

**18.7 A 10Gb/s CMOS CDR and DEMUX IC with a Quarter-Rate Linear Phase Detector** **4:45 PM**

*S. Byun,* Electronics and Telecommunications Research Institute, Daejeon, Korea

A 10Gb/s CDR and DEMUX IC in a 0.13µm CMOS consumes 100mA from a 1.2V core supply and 205mA from a 2.5V I/O supply including 18 LVDS drivers. The CDR system uses a quarter-rate linear phase detector and a 4-phase 2.5GHz LC-QVCO to achieve a BER of $<10^{-15}$ and a jitter tolerance of $0.5UI_{pp}$ exceeding the OC-192 standard.

**18.8 A 20Gb/s Embedded Clock Transceiver in 90nm CMOS** **5:00 PM**

*J. Jaussi,* Intel, Hillsboro, OR

A 20Gb/s embedded clock transceiver in 90nm CMOS is described. The RX front-end is 4-way interleaved with a LC-VCO-based CDR. The random jitter of the recovered clock is $1.44ps_{rms}$. Data transfer rates of 20Gb/s across a 2-inch link and 14.4Gb/s across a 22-inch backplane link are achieved. At 20Gb/s, the transceiver dissipates 15.9mW/Gb/s.